CUSTOMER NO. 23932

PATENT APPLICATION
Docket #61181-14USPX

EXPRESS MAIL Mailing Label No: EV296585704US

Date of Deposit February 26, 2004

Type or Print Name .... CAROL MARTIN

Carol Martin

Signature

GATE VOLTAGE REGULATION SYSTEM FOR A NON-VOLATILE MEMORY CELL PROGRAMMING AND/OR SOFT PROGRAMMING PHASE

PRIORITY CLAIM

The present application claims priority from European Patent Application No. 03425134.8 filed February 28 2003, the disclosure of which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

Technical Field of the Invention

[1] The present invention relates to a gate voltage regulation system for the programming and/or soft programming phase of non volatile memory cells. More particularly, the invention relates to a gate voltage regulation system for the programming and/or soft programming phase of non volatile memory cells, for example of the flash type, with low circuit area occupation.

Description of Related Art

[2] As it is well known in this specific technical field, in modern semiconductor-integrated non volatile memory devices, for example in flash EEPROM memories, the need to apply very "precise" voltages to memory cells in the writing step is increasingly felt. This is generally valid both for writing cells having a grounded bulk terminal, essentially with Vbulk=0, and for negative Vbulk writing.

[3] Writing operations for a Flash memory are essentially of two types:

- real programming, in order to change the logic status of a cell from erased to programmed; and

- soft programming, which is a low efficiency kind of programming required to control more precisely the threshold shift of a given cell.

[4] Usually, a soft programming is necessary after an erasing in order to recover all those bits whose threshold near to zero could cause false reading problems in a NOR memory architecture.

[5] The circuits involved in both the programming and the soft programming operation are essentially the same, differing only in that the voltages required in the soft programming phase are lower than the voltages of the programming phase. More particularly, the following rules quoted in Table 1 are generally valid:

		Programming	Soft Programming
V_{gate}	Ramp	Vstart-p, Vfinal-p, ΔTpulse-p	Vstart-p, Vfinal-p, ΔTpulse-p
V_{drain}	Const.	V_d	V_d
V_{bulk}	Const.	0 or negative	0 or negative
V_{source}	Const.	0	0

Table 1

[6] Essentially, the programming phase is performed by applying a ramp voltage on the memory cell gate terminal, thus ensuring (if performed with a quite precise ramp slope) the desired threshold shift in the desired time and with a constant current. By indicating the voltage values at the ramp beginning and end with the references Vstart and Vfinal and the ramp duration with Tprogram, a constant current programming is obtained, as shown in FIGURE 1.

[7] The ramp can be generally formed in two ways:

- analogue; which is obtained by means of a linear ramp; and

- through pulses; which is obtained by means of several short pulses in order to interpolate the linear feature.

[8] The problems linked to the creation of a pulse ramp will now be considered. Such a voltage ramp must be linear with values Vstart, Vfinal, Tpulse=Tprogram being as independent as possible from operating conditions, such as for example:

- Vsupply, memory device supply voltage;

- operating temperature; and

- capacitive load change

[9] It is not simple at all to manufacture a circuitry which succeeds, with low area occupation, in ensuring a constant ramp when the above-mentioned operating conditions vary. Moreover, once the regulation system to be used is defined and fixed, it does not mean that it equally suits both the programming and the soft programming phase.

[10] The potential limits of a single regulation system will be examined first. The problems linked to the use of a single regulation system for both phases will be briefly analyzed.

[11] Programming: in this case the voltage ramp, starting from low values being almost equal to the supply voltage for 3V-operating memories is brought to values near to technology-supportable values, for example ~10V. In this case it is necessary to form a ramp as near as possible to the ideal ramp, but without having a series regulator, since the voltage difference ΔV required at the regulator series transistor terminals would lead to an upstream voltage being dangerously near, if not even higher than the borderline voltage provided by the technology.

[12] Referring to what has been described above, FIGURE 2A, showing a threshold voltage distribution of memory array cells, can be observed. The programmed cell distribution is indicated with D2. The cell distribution after erasing is indicated with D1. Cells to be recovered after the erasing operation are in grey.

[13] Similarly, FIGURE 2B shows a threshold voltage distribution of the cells of a memory array wherein cells being over-recovered after the erasing operation are represented in percentage in grey, in the case of a high efficiency charge pump.

[14] Generally, it is preferable to connect the charge pump output, responsible for the voltage ramp creation, directly to the gate node, by using an ON/OFF regulation. In this case problems are those linked to the pump efficiency. In fact, as shown in FIGURE 3, in the ramp lower part, at low voltages, a high pump efficiency occurs, but this could lead to serious regulation problems intended as a ripple which cannot be easily controlled, and thus to a distorted ramp trend very far from being ideal. If the pump efficiency is to be decreased, serious problems could arise in the ramp upper part, where the pump would have difficulty to follow the ideal ramp, as shown in FIGURE 4.

[15] Soft Programming: in this case the problem is even more serious. In fact the charge pump operates at even lower voltage values, generally lower than supply voltages for a 3V-powered memory device. Therefore, the ripple management becomes in this case very demanding.

[16] The technical problem underlying the present invention is to provide a gate voltage regulation system, particularly for the programming and soft programming phase of non volatile memory cells, having such structural and functional characteristics as to improve the voltage regulator answer fidelity at low voltages, overcoming the limits of present prior art solutions.

SUMMARY OF THE INVENTION

[17] The present invention solves the foregoing and other problems by providing gate voltage regulation circuits that are structurally and functionally independent, with one responsible for the programming phase and another responsible for the soft programming phase.

[18] In accordance with one embodiment of the invention, a gate voltage regulation system performs programming and/or soft programming of non volatile memory cells. The memory cells are organized in cell matrices with corresponding circuits responsible for addressing, decoding, reading, writing and erasing the memory cell content. The system includes charge pump voltage regulators for biasing gate terminals of the cells in the programming phase with a predetermined voltage value. A first regulation stage and a second regulation stage, which are structurally independent, are responsible for the programming phase and soft programming phase, respectively. The first stage generates a supply voltage for the second stage.

[19] In accordance with another embodiment of the invention, a circuit includes a first and second voltage regulation stage. The first voltage regulation stage generates a voltage ramp output at a first output. The second voltage regulation stage generates a regulated voltage output at a second output. A selection switch responds to a control signal to selectively connect the first output to the second output.

[20] In accordance with another embodiment of the invention, a circuit includes a plurality of volatile memory cells, each including a transistor, and each of the transistors sharing a common gate connection. A gate voltage regulator circuit includes an output coupled to the common gate connection and receives a programming control signal. The gate voltage regulator circuit comprises and first and second regulator. The first regulator generates a programming ramp voltage and the second regulator generates a soft programming voltage. A selection circuit responds to the programming control signal and applies the programming ramp voltage to the

common gate connection in a first operating mode and applies only the soft programming voltage to the common gate connection in a second operating mode.

BRIEF DESCRIPTION OF THE DRAWINGS

[21] A more complete understanding of the method and apparatus of the present invention may be acquired by reference to the following Detailed Description when taken in conjunction with the accompanying Drawings wherein:

[22] FIGURE 1 schematically shows the voltage trend at the beginning and at the end of a constant current programming ramp;

[23] FIGURE 2A schematically shows a diagram illustrating a threshold voltage distribution of memory cells in a cell array; the programmed cell distribution is indicated with D2 while the cell distribution after the erasing is indicated with D1; cells to be recovered after the erasing operation are in grey;

[24] FIGURE 2B schematically shows a diagram illustrating a distribution of erased memory cells in a cell array; cells being over-recovered after the erasing operation are represented in percentage in grey, in the case of a high efficiency charge pump;

[25] FIGURE 3 schematically shows a diagram voltage vs. time comparing an ideal ramp (broken line) to a real ramp (bold print) in the case of a high efficiency charge pump;

[26] FIGURE 4 schematically shows a diagram voltage vs. time comparing an ideal ramp (broken line) to a real ramp (bold print) in the case of a low efficiency charge pump;

[27] FIGURE 5 schematically shows a regulation system according to the present invention for generating the gate voltage, particularly for the Programming and soft programming phase of non volatile memory cells; and

[28] FIGURE 6 schematically shows a memory cell array associated to the regulation system of FIGURE 5.

DETAILED DESCRIPTION OF THE DRAWINGS

[29] With reference to the figures, a gate voltage regulation system for the programming and/or soft programming phase of non volatile memory cells, for example of the flash type, with low circuit area occupation, is globally and schematically indicated with reference 1.

[30] Non volatile memories are electronic devices integrated on semiconductor and equipped with memory cell matrices, particularly multilevel cells. More particularly, memory device means any monolithic electronic system incorporating a matrix 5 of memory cells 9, organized in rows, referred to as word lines 10, and columns, referred to as bit lines 11, as well as circuit portions associated to the cell matrix and responsible for the functions of addressing, decoding, reading, writing and erasing the memory cell content. Such a matrix 5 is shown for example in FIGURE 6. Such a device can be, for example, a memory chip integrated on semiconductor and of the non volatile EEPROM Flash type which is split in sectors and is electrically erasable.

[31] Each memory cell comprises a floating gate transistor with source S, drain D and control gate G terminals. Among the circuit portions associated to the cell matrix programming

circuits are provided, which are associated to the gate G terminals of the memory cells and supplied with a specific supply voltage Vdd applied to a charge pump circuit portion 6. Moreover, a voltage regulator 7 is provided for the charge pump circuit portion 6. In the example of FIGURE 5 the charge pump 6 is supplied with the voltage Vdd and regulated by the output of the stable voltage regulator 7 which operates by drawing a stable voltage reference Vref.

[32] Circuit portions 6 and 7 belong to a first regulation circuit or stage ST1 which, according to the present invention, is responsible for the creation and regulation of a voltage ramp to be applied to the gate terminals of memory cells in the programming phase. This first stage ST1 has an output 3 inputted to a second regulation circuit or stage ST2. The circuit further includes a second stage ST2 which is responsible for the creation and regulation of a voltage ramp to be applied to the gate terminals of memory cells in the soft programming phase.

[33] Advantageously, according to the present invention, the circuitry responsible for the programming and soft programming operations has been differentiated from prior art solutions and with respect to the kind of operation being performed. In the soft programming case, instead of applying the charge pump voltage directly to the cell terminals, a regulated voltage is applied, which exploits the charge pump output as supply line.

[34] Essentially, the system according to the invention comprises at least two main stages:

- a first coarse voltage regulation stage ST1; and

- a second precise regulation stage ST2.

[35] The second stage ST2 comprises a current mirror circuit structure 2 having a transistor circuit branch coupled between the output 3 of the first stage ST1 and a ground potential reference, as well as a second transistor circuit branch coupled to the gate terminals of cells 5. In parallel to the second circuit branch an enabling transistor 4 is provided, which receives, on the control terminal thereof, a signal Softp to control the switching of the circuit operation to a soft programming phase.

[36] A gate voltage regulator 8, receiving a voltage reference Vref, is provided to voltage-drive the gate terminal of a transistor of the second circuit branch of the current mirror structure 2. The charge pump output 6 supplies thus the current mirror structure 2 as if it were a real power supply or supply line. A transistor 12 operating in saturation conditions is provided between the voltage produced by the pump 6 output and the voltage being applied to the gate terminals of memory cells 5 through the current mirror.

[37] The system 1 remains of the ON/OFF type in which the stage ST1 upper node is regulated by a voltage Vdd being higher than the voltages commonly used in soft programming, for example the reading voltage of 4 – 5 V.

[38] Since the current mirror structure 2 comprises transistors having known area and size, it is thus possible to set conveniently the charge current of node 13.

[39] The transistor 4 inserted between the pump 6 and the node to be regulated, operating in saturation, will thus absorb all voltage changes due to pump boost changes, protecting downstream circuits which will be instead constant-current-supplied.

[40] Very briefly, it can be said that the regulation system according to the invention exploits a current mirror supplied with a coarse regulated voltage. In other words, the operation

in saturation of transistor 12 allows voltage changes between nodes 3 and 13 to be absorbed, due to the output features of a transistor operating in saturation, in practice when 3, 13 vary, the current Isource=constant and thus the node 13 charge always occurs in a controlled way.

[41] Although preferred embodiments of the method and apparatus of the present invention have been illustrated in the accompanying Drawings and described in the foregoing Detailed Description, it will be understood that the invention is not limited to the embodiments disclosed, but is capable of numerous rearrangements, modifications and substitutions without departing from the spirit of the invention as set forth and defined by the following claims.